IN THE CLAIMS

Claims 1, 2 and 5 through 8 are pending in this application. Please cancel Claims 3, 4 and 9 through 11 without prejudice or disclaimer, and please amend Claims 1, 2 and 5 through 8, as follows:

1. (Currently Amended) A multichip module including a module substrate having plural wiring layers, ~~many~~ a plurality of external connecting electrodes formed on one face of said module substrate, and a plurality of mounting pads ~~pad~~ for mounting ~~plural~~ a plurality of semiconductor integrated circuit chips formed on the other face of said module substrate;

wherein an area of said module substrate allocated to said plurality of mounting ~~pad~~ pads is separated into an area ~~of the~~ for a mounting pad ~~of the plural~~ for semiconductor integrated circuit chips ~~able to be relatively~~ operated at relatively high speed, and an area ~~of the~~ for a mounting pad ~~of the plural~~ for semiconductor integrated circuit chips operated at relatively low speed[,] [;] ~~and~~

wherein external connecting electrodes of the plurality of external connecting electrodes ~~corresponding to~~ for [an] address outputs ~~output~~ and [a] data inputs-outputs ~~input-output~~ are arranged on a rear face of said module substrate corresponding to said area for the mounting pad for semiconductor integrated circuit chips operated at relatively low speed on a front face of said module substrate for mounting the ~~plural~~ semiconductor integrated circuit chips operated at relatively low speed[.], and

wherein said area for the mounting pad for semiconductor integrated circuit chips operated at relatively low speed on the front face of said module substrate is coupled to the external connecting electrodes of said plurality of external connecting electrodes for said address outputs and said data inputs-outputs operated at relatively low speed.

2. (Currently Amended) A multichip module according to claim 1, wherein ~~relatively many~~ external connecting electrodes of the plurality of external connecting electrodes allocated to the supply of a power voltage and a ground voltage are arranged on [a] the rear face of said module substrate corresponding to said area for the mounting pad for semiconductor integrated circuit chips operated at relatively high speed on the front face of said module substrate ~~of said area~~ for mounting the ~~plural~~ semiconductor integrated circuit chips operated at relatively high speed.

3-4. (Cancelled)

5. (Currently Amended) A multichip module including a module substrate having a plurality of ~~plural~~ wiring layers, ~~many~~ a plurality of external connecting electrodes formed on one face of said module substrate, a mounting pad formed on the other face of said module substrate, and a data processor chip, a memory chip and a buffer circuit arranged on said module substrate through said mounting pad;

wherein ~~relatively many~~ external connecting electrodes of the plurality of external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of said module substrate corresponding to [of] an area on the front face of said module substrate for mounting said memory chip.

6. (Currently Amended) A multichip module including a module substrate having a plurality of ~~plural~~ wiring layers, ~~many~~ a plurality of external connecting electrodes formed on one face of said module substrate, a mounting pad formed on the other face of said module substrate, and a plurality of ~~plural~~ kinds of semiconductor integrated circuit chips mounted through said mounting pad on the front face of said module substrate;

wherein [the] external connecting electrodes of the plurality of external connecting electrodes for operating power allocated to supply a power voltage and a ground voltage are partly coarsely and partly closely arranged on the module substrate,

and are closely arranged [on] to the rear faces of the semiconductor integrated circuit chips of the plurality of kinds of semiconductor integrated circuit chips having larger power consumption.

7. (Currently Amended) A semiconductor module in which ~~plural~~ a plurality of external connecting electrodes are arranged on one face of a module substrate and a mounting pattern is formed on the other face of the module substrate,[;]

wherein said mounting pattern includes a grouped pattern ~~able to arrange~~ for arranging semiconductor integrated circuit chips of the same kind in a group ~~approximately having an equal height size in one line~~ and for mounting each group of ~~mount these~~ semiconductor integrated circuit chips of the same kind as a group for every group of the semiconductor integrated circuit chips of the same kind ,[;] and

wherein the mounting pattern and ~~a bump electrode~~ said plurality of external connecting electrodes ~~of the semiconductor integrated circuit chip~~ are electroconductively ~~connected~~ coupled to each other through an anisotropic electroconductive film, with each grouped pattern for arranging semiconductor integrated circuit chips of the same kind in a group being electroconductively coupled to said plurality of external connecting electrodes through a corresponding anisotropic electroconductive film ~~stuck every said grouped pattern~~.

8. (Currently Amended) An electronic circuit including a first semiconductor device and a second semiconductor device, with the second semiconductor device for operation at a relatively ~~able to be operated at~~ high speed in comparison with the operation speed of said first semiconductor device, and wherein the first semiconductor device and the second semiconductor device ~~devices~~ are mounted to a bus of a multilayer wiring substrate in a common connecting state;

wherein said second semiconductor device has a data processor chip and a memory chip commonly connected to said bus through ~~an~~ a plurality of external connecting electrodes ~~electrode~~ in [a] the multilayer wiring substrate, and

wherein external connecting electrodes of said plurality of external connecting electrodes allocated to supply a power voltage and a ground voltage are arranged on the rear face of said multilayer wiring substrate corresponding to an area on the front face of said multilayer wiring substrate for mounting said memory chip.

~~and includes a buffer circuit in a wiring path from said data processor chip and the memory chip to said external connecting electrode;~~

~~said buffer circuit interrupts an input from said bus in access of the memory chip using said data processor chip; and~~

~~the external connecting electrode allocated for an address and data is arranged on the rear face of an area for mounting said buffer circuit.~~

9-11. (Cancelled)